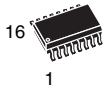
M41T315Y
M41T315V, M41T315W

Serial access phantom RTC supervisor

Not For New Design

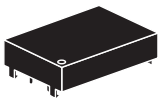
Features

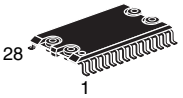
- 3.0V, 3.3V, or 5V operating voltage
- Real-time clock keeps track of tenths/hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Automatic leap year correction valid up to 2100
- Automatic switch-over and deselect circuitry
- Choice of power-fail deselect voltages: (V_{PFD} = power-fail deselect voltage)
  - M41T315Y[(a)]: V_{CC} = 4.5 to 5.5V
    $4.25V \le V_{PFD} \le 4.50V$
  - M41T315V: V_{CC} = 3.0 to 3.6V
    $2.80V \le V_{PFD} \le 2.97V$
  - M41T315W: V_{CC} = 2.7 to 3.3V
    $2.60V \le V_{PFD} \le 2.70V$
- No address space required to communicate with RTC
- Provides nonvolatile supervisor functions for battery backup of SRAM
- Full ±10% V_{CC} operating range
- Industrial operating temperature range (–40 to +85°C)
- Ultra-low battery supply current of 500nA (max)
- Optional packaging includes A 28-lead SOIC and SNAPHAT® top (to be ordered separately)
- SNAPHAT package provides direct connection for a snaphat top, which contains the battery and crystal
- RoHS compliant
  - Lead-free second level interconnect



SO16 (MQ)

SNAPHAT (SH)
battery & crystal





SOH28 (MH)

a. Contact local ST sales office for availability.

This is information on a product still in production but not recommended for new designs. www.st.com

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1 Description

The M41T315Y/V/W RTC Supervisor is a combination of a CMOS TIMEKEEPER® and a nonvolatile memory supervisor. Power is constantly monitored by the memory supervisor. In the event of power instability or absence, an external battery maintains the timekeeping operation and provides power for a CMOS static RAM by switching on and invoking write protection to prevent data corruption in the memory and RTC.

The clock keeps track of tenths/hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The last day of the month is automatically adjusted for months with less than 31 days, including leap year correction.

The clock operates in one of two formats:

- a 12-hour mode with an AM/PM indicator;

or

- a 24-hour mode

The nonvolatile supervisor supplies all the necessary support circuitry to convert a CMOS RAM to a nonvolatile memory. The M41T315Y/V/W can be interfaced with RAM without leaving gaps in memory.

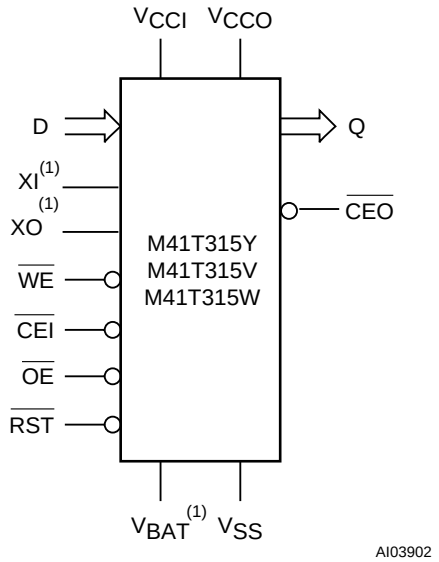
The M41T315Y/V/W is supplied in a 28-lead SOIC SNAPHAT® package (which integrates both crystal and battery in a single SNAPHAT top) or a-16 pin SOIC. The 28-pin, 330mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT housing containing the battery and crystal. The unique design allows the SNAPHAT battery/crystal package to be mounted on top of the SOIC package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is also keyed to prevent reverse insertion.

The 28-pin SOIC and battery/crystal packages are shipped separately in plastic anti-static tubes or in Tape & Reel form. For the 28-lead SOIC, the battery/crystal package (e.g., SNAPHAT) part number is “M4TXX-BR12SH” (see *Table 17 on page 28*).

Caution: Do not place the SNAPHAT battery/crystal top in conductive foam, as this will drain the lithium button-cell battery.

Figure 1. Logic diagram



1. For 16-pin SOIC only

Table 1. Signal names

XI-XO	32.768 KHz crystal connection
D	Data input
Q	Data output
$\overline{RST}$	Reset input
$\overline{CEO}$	Chip enable output
$\overline{CEI}$	Chip enable input
V_{BAT}	Battery input
$\overline{OE}$	Output enable input
$\overline{WE}$	WRITE enable input
V_{CCO}	Switched supply voltage output
V_{CCI}	Supply voltage input
V_{SS}	Ground
NC	Not connected internally
DU	Don't Use

Figure 2. 16-pin SOIC connections

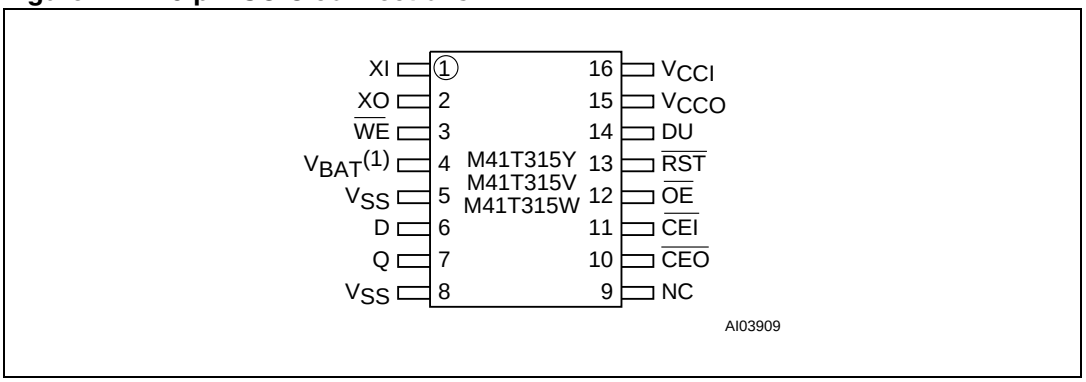


Figure 3. 28-pin SOIC connections

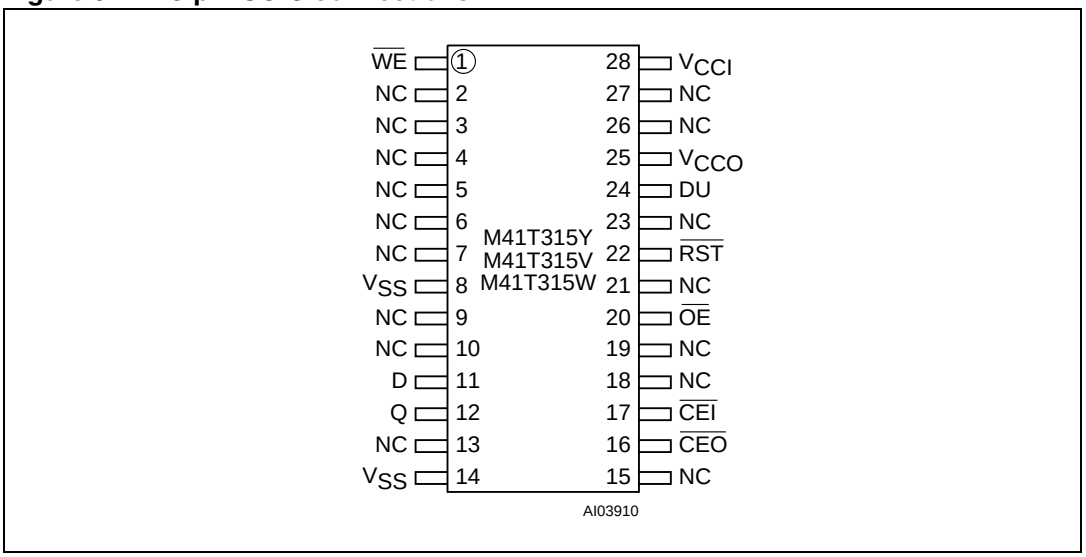


Figure 4. Block diagram

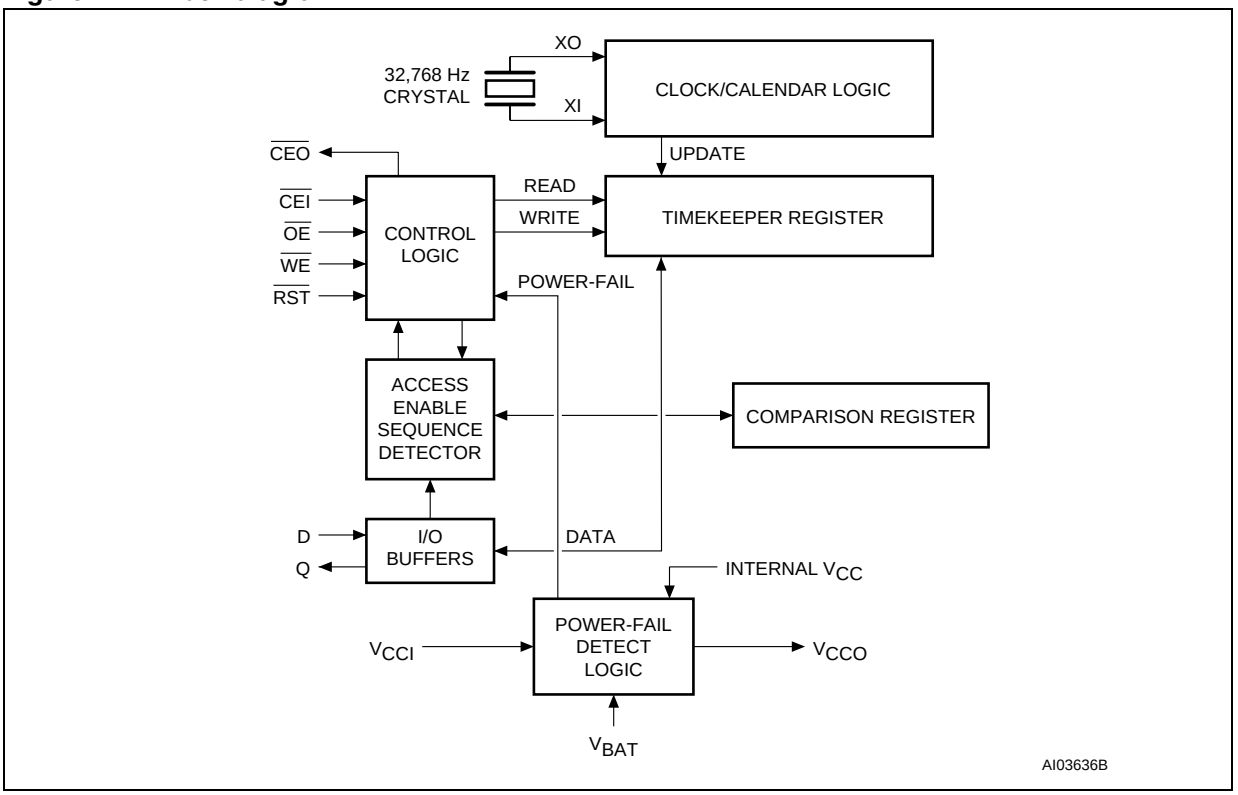
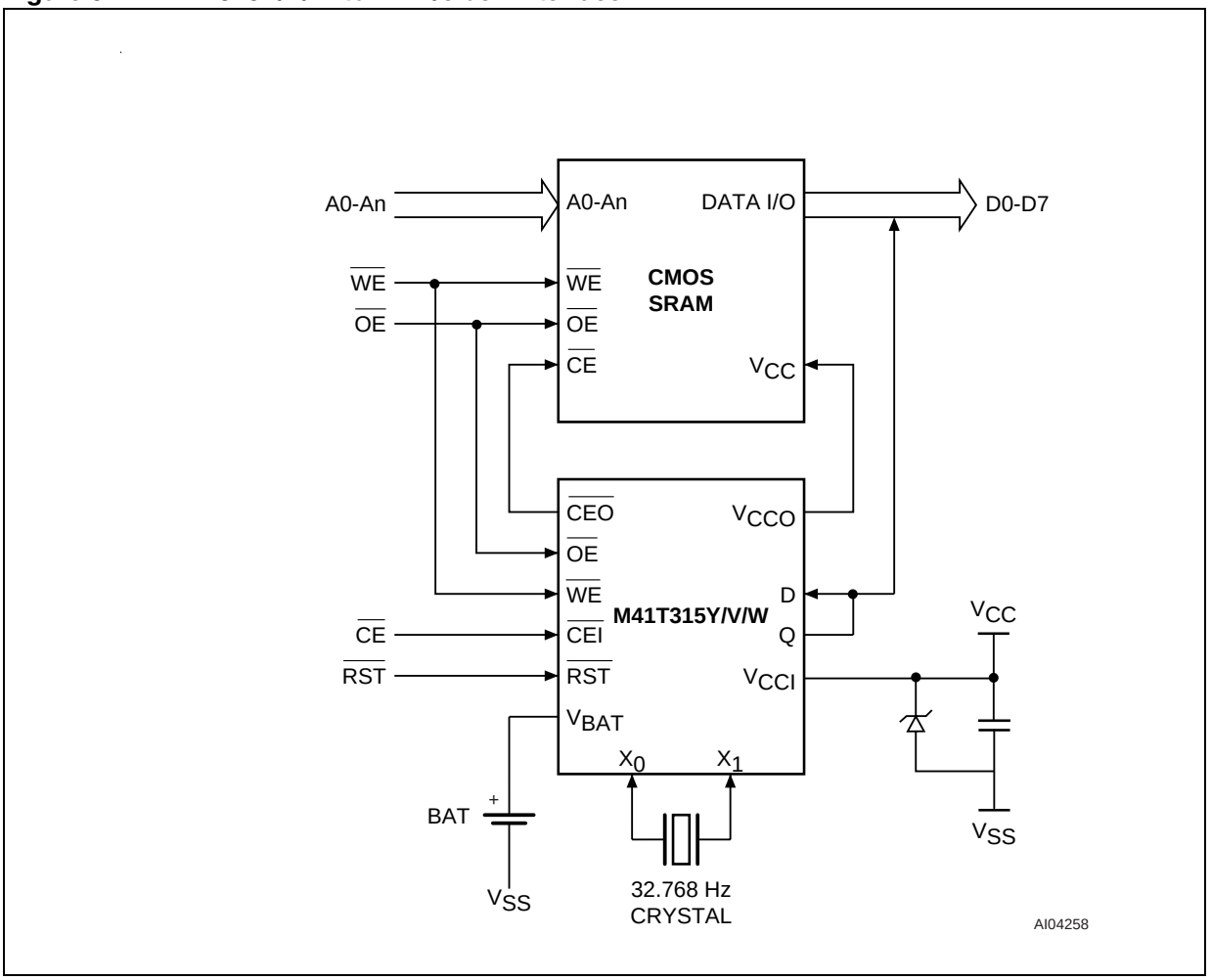


Figure 5. M41T315Y/V/W to RAM/clock interface



2 Operation

Figure 6 on page 11 illustrates the main elements of the device. The following paragraphs describe the signals and functions.

Communication with the clock is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive WRITE cycles containing the proper data on data in (D). All accesses which occur prior to recognition of the 64-bit pattern are directed to memory via the chip enable output pin ($\overline{CEO}$).

After recognition is established, the next 64 READ or WRITE Cycles either extract or update data in the clock and $\overline{CEO}$ remains high during this time, disabling the connected memory (see *Table 2 on page 11*).

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of chip enable input ($\overline{CEI}$), output enable ($\overline{OE}$), and WRITE enable ($\overline{WE}$). Initially, a READ cycle using the $\overline{CEI}$ and $\overline{OE}$ control of the clock starts the pattern recognition sequence by moving the pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive WRITE cycles are executed using the $\overline{CEI}$ and $\overline{WE}$ control of the clock. These 64 WRITE cycles are used only to gain access to the clock.

When the first WRITE cycle is executed, it is compared to the first bit of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next WRITE cycle.

If a match is not found, the pointer does not advance and all subsequent WRITE cycles are ignored. If a READ cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 WRITE cycles as described above until all the bits in the comparison register have been matched (see *Figure 8 on page 14*).

With a correct match for 64 bits, access to the registers is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the device to either receive data on D, or transmit data on Q, depending on the level of $\overline{OE}$ pin or the WE pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CEI}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the device.

For a SO16 pin package, a standard 32.768 kHz quartz crystal can be directly connected to the M41T315Y/V/W via pins 1 and 2 (XI, XO). The crystal selected for use should have a specified load capacitance (C_L) of 12.5 pF (see *Table 10 on page 21*).

Table 2. Operating modes

Mode	V_{CC}	$\overline{CEI}$	$\overline{OE}$	$\overline{WE}$	D	Q	Power
Deselect	4.5 to 5.5V or 3.0 to 3.6V or 2.7 to 3.3V	V_{IH}	X	X	Hi-Z	Hi-Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Hi-Z	Active
READ		V_{IL}	V_{IL}	V_{IH}	Hi-Z	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	Hi-Z	Hi-Z	Active
Deselect	V_{SO} to V_{PFD} (min)(1)	X	X	X	Hi-Z	Hi-Z	CMOS standby
Deselect	$\leq V_{SO}$(1)	X	X	X	Hi-Z	Hi-Z	Battery back-up mode

1. See *Table 11 on page 21* for details.

2.1 Non-volatile supervisor operation

A switch is provided to direct power from the battery input or V_{CCI} to V_{CCO} with a maximum voltage drop of 0.3 Volts. The V_{CCO} output pin is used to supply uninterrupted power to CMOS SRAM. The M41T315Y/V/W safeguards the clock and RAM data by power-fail detection and write protection.

Power-fail detection occurs when V_{CCI} falls below V_{PFD} which is set by an internal bandgap reference. The M41T315Y/V/W constantly monitors the V_{CCI} supply pin. When V_{CCI} is less than V_{PFD}, power-fail circuitry forces the chip enable output ($\overline{CEO}$) to V_{CCI} or V_{BAT}-0.2 volts for external RAM write protection. During nominal supply conditions, $\overline{CEO}$ will track $\overline{CEI}$ with a propagation delay. Internally, the M41T315Y/V/W aborts any data transfer in progress without changing any of the device registers and prevents future access until V_{CCI} exceeds V_{PFD}. *Figure 5 on page 9* illustrates a typical RAM/clock interface.

Figure 6. Read mode waveforms

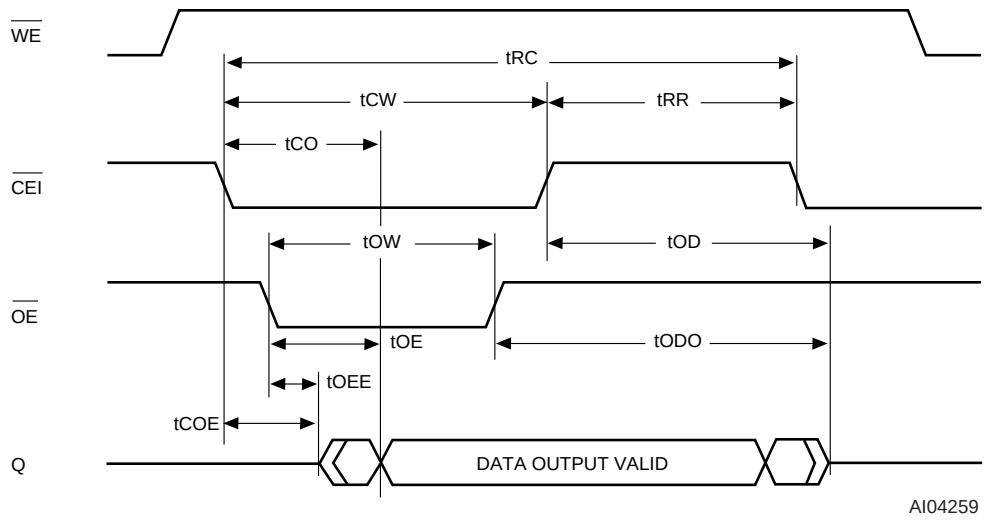


Figure 7. Write mode waveforms

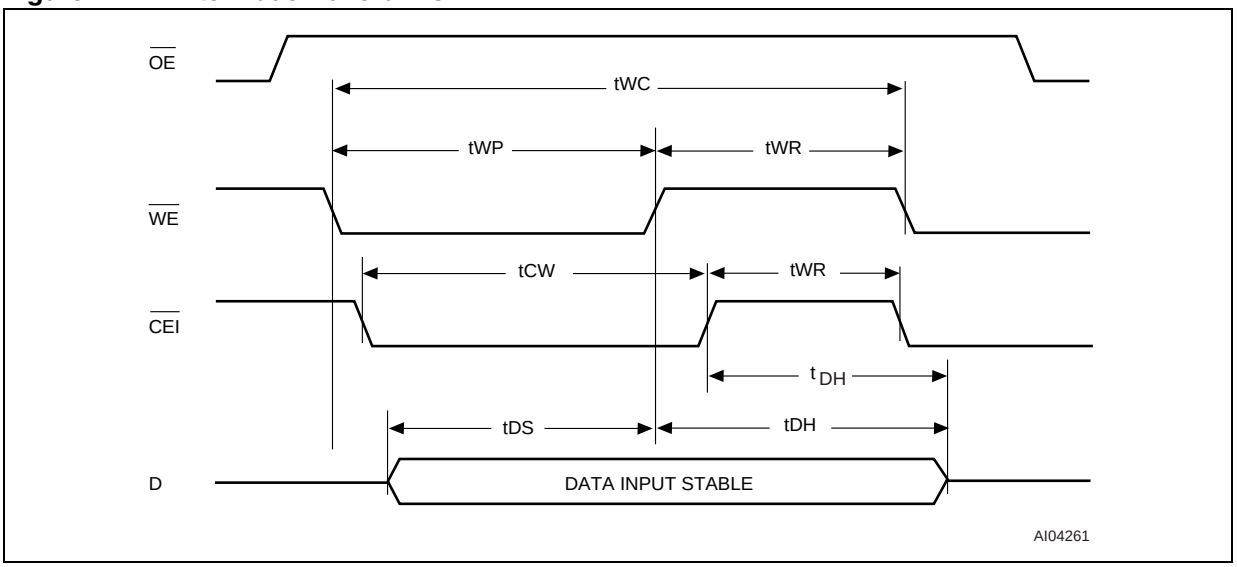


Table 3. AC electrical characteristics (M41T315Y)

Symbol		Parameter[1]	Min	Typ	Max	Units
t_{AVAV}	t_{RC}	READ cycle time	65			ns
t_{ELQV}	t_{CO}	$\overline{CEI}$ access time			55	ns
t_{GLQV}	t_{OE}	$\overline{OE}$ access time			55	ns
t_{ELQX}	t_{COE}	$\overline{CEI}$ to output low Z	5			ns
t_{GLQX}	t_{OEE}	$\overline{OE}$ to output low Z	5			ns
t_{EHQZ}	t_{OD}	$\overline{CEI}$ to output high Z			25	ns
t_{GHQZ}	t_{ODO}	$\overline{OE}$ to output high Z			25	ns
	t_{RR}	READ recovery	10			ns
t_{ELEH}	t_{CW}	$\overline{CEI}$ pulse width	55			ns
t_{GLGH}	t_{OW}	$\overline{OE}$ pulse width	55			ns
t_{AVAV}	t_{WC}	WRITE cycle	65			ns
t_{WLWH}	t_{WP}	WRITE pulse width	55			ns
t_{EHAX} t_{WHAX}	t_{WR}[2]	WRITE recovery	10			ns
t_{DVEH} t_{DVWH}	t_{DS}[3]	Data setup	30			ns
t_{EHDX} t_{WHDX}	t_{DH}[3]	Data hold time	0			ns
	t_{RST}	$\overline{RST}$ pulse width	65			ns

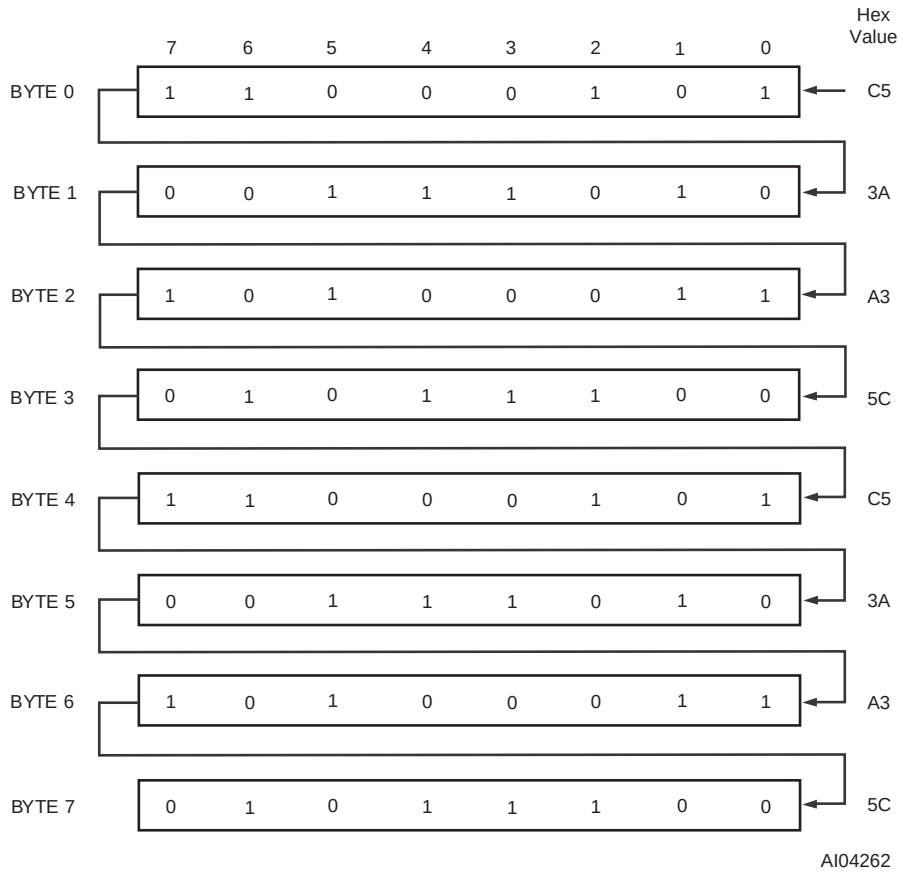
1. Valid for ambient operating temperature: TA = –40 to 85°C; VCC = 4.5 to 5.5V (except where noted).
2. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CEI}$.
3. t_{DH} and t_{DS} are functions of the first occurring edge of $\overline{WE}$ or $\overline{CEI}$ in RAM mode.

Table 4. AC electrical characteristics (M41T315V/W)

Symbol		Parameter[1]	Min	Typ	Max	Units
t_{AVAV}	t_{RC}	READ cycle time	85			ns
t_{ELQV}	t_{CO}	$\overline{CEI}$ access time			85	ns
t_{GLQV}	t_{OE}	$\overline{OE}$ access time			85	ns
t_{ELQX}	t_{COE}	$\overline{CEI}$ to output low Z	5			ns
t_{GLQX}	t_{OEE}	$\overline{OE}$ to output low Z	5			ns
t_{EHQZ}	t_{OD}	$\overline{CEI}$ to output high Z			30	ns
t_{GHQZ}	t_{ODO}	$\overline{OE}$ to output high Z			30	ns
	t_{RR}	READ recovery	20			ns
t_{ELEH}	t_{CW}	$\overline{CEI}$ pulse width	65			ns
t_{GLGH}	t_{OW}	$\overline{OE}$ pulse width	60			ns
t_{AVAV}	t_{WC}	WRITE cycle	85			ns
t_{WLWH}	t_{WP}	WRITE pulse width	60			ns
t_{EHAX} t_{WHAX}	t_{WR}[2]	WRITE recovery	25			ns
t_{DVEH} t_{DVWH}	t_{DS}[3]	Data setup	35			ns
t_{EHDX} t_{WHDX}	t_{DH}[3]	Data hold time	5			ns
	t_{RST}	$\overline{RST}$ pulse width	85			ns

1. Valid for ambient operating temperature: TA = –40 to 85°C; VCC = 4.5 to 5.5V (except where noted).
2. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CEI}$.
3. t_{DH} and t_{DS} are functions of the first occurring edge of $\overline{WE}$ or $\overline{CEI}$ in RAM mode.

Figure 8. Comparison register definition



Note: Pattern recognition in "hex" is C5, 3A, A3, 5C, C5, 3A, A3, and 5C. The odds of this pattern being accidentally duplicated and sending aberrant entries to the RTC is less than 1 in 10^{19}. This pattern is sent to the clock LSB to MSB.

2.2 Data retention

Most low power SRAMs on the market today can be used with the M41T315Y/V/W. There are, however some criteria which should be used in making the final choice of an SRAM to use. The SRAM must be designed in a way where the chip enable input disables all other inputs to the SRAM. This allows inputs to the M41T315Y/V/W and SRAMs to be Don't Care once V_{CCI} falls below V_{PFD}(min). The SRAM should also guarantee data retention down to V_{CC} = 2.0 volts. The chip enable access time must be sufficient to meet the system needs with the chip enable output propagation delays included. If the SRAM includes a second chip enable pin (E2), this pin should be tied to V_{OUT}.

If data retention lifetime is a critical parameter for the system, it is important to review the data retention current specifications for the particular SRAMs being evaluated. Most SRAMs specify a data retention current at 3.0 volts. Manufacturers generally specify a typical condition for room temperature along with a worst case condition (generally at elevated temperatures). The system level requirements will determine the choice of which value to

use. The data retention current value of the SRAMs can then be added to the IBAT value of the M41T315Y/V/W to determine the total current requirements for data retention. The available battery capacity for the SNAPHAT® of your choice can then be divided by this current to determine the amount of data retention available (see *Table 17 on page 28*).

For a further more detailed review of lifetime calculations, please see Application Note AN1012.

3 Clock operation

3.1 Clock register information

Clock information is contained in eight registers of 8 bits, each of which is sequentially accessed 1 bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the clock registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These READ/WRITE registers are defined in *Table 5 on page 17*.

Data contained in the clock registers is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping though all eight registers, starting with Bit 0 of Register 0 and ending with Bit 7 of Register 7.

3.2 AM-PM/12/24 mode

Bit 7 of the hours register is defined as the 12-hour or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, Bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, Bit 5 is the second 10-hour bit (20-23 hours).

3.3 Oscillator and reset bits

Bits 4 and 5 of the day register are used to control the reset and oscillator functions. Bit 4 controls the reset pin input. When the Reset Bit is set to logic '1,' the reset input pin is ignored. When the Reset Bit is set to logic '0,' a low input on the reset pin will cause the device to abort data transfer without changing data in the timekeeping registers. Reset operates independently of all other inputs. Bit 5 controls the oscillator. When set to logic '0,' the oscillator turns on and the real-time clock/calendar begins to increment.

3.4 Zero bits

Registers 1, 2, 3, 4, 5, and 6 contain one (1) or more bits that will always read logic '0.' When writing to these locations, either a logic '1' or '0' is acceptable.

Table 5. RTC register map

Register	D7	D6	D5	D4	D3	D2	D1	D0	Function/range BCD format	
0	0.1 seconds				0.01 seconds				seconds	00-99
1	0	10 seconds			seconds				seconds	00-59
2	0	10 minutes			minutes				minutes	00-59
3	12/24	0	10/ A/P	hrs	hours (24 hour format)				hours	01-12/ 00-23
4	0	0	$\overline{OSC}$	$\overline{RST}$	0	day of the week			day	01-07
5	0	0	10 date		date: day of the month				date	01-31
6	0	0	0	10M	month				month	01-12
7	10 years				year				year	00-99

Keys:

A/P = AM/PM bit

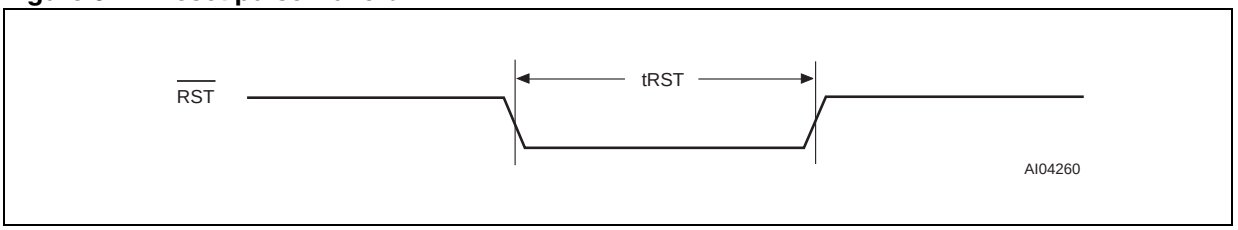
12/24 = 12 or 24-hour mode bit

$\overline{OSC}$ = Oscillator bit

$\overline{RST}$ = Reset bit

0 = Must be set to ‘0’

Figure 9. Reset pulse waveform



4 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Ablolute maximum ratings

Symbol	Parameter		Value	Unit
T_A	Operating temperature		–40 to +85	°C
T_{STG}	Storage temperature (V_{CC}, oscillator off)	SNAPHAT®	–40 to +85	°C
		SOIC	–55 to +125	°C
T_{SLD}(1)	Lead solder temperature for 10 seconds		260	°C
V_{CCI}	Supply voltage (on any pin relative to Ground)	M41T315Y	–0.3 to +7.0	V
		M41T315V/W	–0.3 to +4.6	V
V_{IO}	Input or output voltages		–0.3 to V_{CC} to +0.3	V
I_O	Output current		20	mA
P_D	Power dissipation		1	W

1. For SO package, Lead-free (Pb-free) lead finish: Reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).

Caution: Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.

Caution: Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.

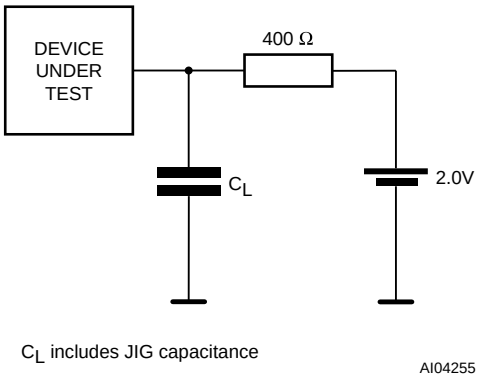
5 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 7. DC and AC measurement conditions

Parameter	M41T315Y	M41T315V/W
V_{CC} supply voltage	4.5 to 5.5V	2.7 to 3.6V
Ambient operating temperature	–40 to +85°C	–40 to +85°C
Load capacitance (C_L)	100pF	50pF
Input rise and fall times	≤ 5ns	≤ 5ns
Input pulse voltages	0 to 3V	0 to 3V
Input and output timing ref. voltages	1.5V	1.5V

Figure 10. AC testing load circuit



Note: 50pF for M41T315V.

Table 8. Capacitance

Symbol	Parameter(1)(2)	Min	Max	Unit
C_{IN}	Input capacitance		10	pF
C_{IO}(3)	Input/output capacitance		10	pF

1. Effective capacitance measured with power supply at 5V; sampled only; not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs were deselected.

Table 9. DC characteristics

Sym	Parameter	Test condition(1)	M41T315Y			M41T315V/W			Unit
			–65			–85			
			Min	Typ	Max	Min	Typ	Max	
I_{IL}(2)	Input leakage current	$0V \le V_{IN} \le V_{CC}$			±1			±1	µA
I_{OL}	Output leakage current	$0V \le V_{OUT} \le V_{CC}$			±1			±1	µA
I_{CC1}(3)	Supply current				10			6	mA
I_{CCO1}(4)	V_{CC} power supply current	$V_{CC0} = V_{CC1} - 0.3$			150			100	mA
I_{CC2}(3)	Supply current (TTL standby)	$\overline{CEI} = V_{IH}$			3			2	mA
I_{CC3}(3)	V_{CC} power supply current	$\overline{CEI} = V_{CC1} - 0.2$			1			1	mA
V_{IL}(5)	Input low voltage		–0.3		0.8	–0.3		0.6	V
V_{IH}(5)	Input high voltage		2.2		V_{CC1} + 0.3	2.0		V_{CC} + 0.3	V
V_{OL}(6)	Output low voltage	I_{OL} = 4.0 mA			0.4			0.4	V
V_{OH}(6)	Output high voltage	I_{OH} = –1.0 mA	2.4			2.4			V
V_{PFD}	Power fail deselect		4.25		4.50	2.80 (V) 2.60 (W)		2.97 (V) 2.70 (W)	V
V_{SO}	Battery back-up switchover			V_{BAT}			2.5		V
V_{BAT}	Battery voltage		2.5		3.7	2.5		3.7	V
V_{CEO}	$\overline{CEO}$ output voltage		V_{CC1} – 0.2 or V_{BAT} – 0.2			V_{CC1} – 0.2 or V_{BAT} – 0.2			V
I_{BAT}(3)	Battery current	V_{BAT} = 3.0V T_A = 25°C V_{CC} = 0V			0.5			0.5	µA
I_{CCO2}(7)	Battery backup current	$V_{CC0} = V_{BAT} - 0.2V$			100			100	µA

1. Valid for ambient operating temperature: TA = –40 to 85°C; VCC = 4.5 to 5.5V or 2.7 to 3.6V (except where noted).
2. Applies to all input pins except $\overline{RST}$, which is pulled internally to V_{CCI}.
3. Measured without RAM connected.
4. ICCO1 is the maximum average load current the device can supply to external memory.
5. Voltages are referenced to Ground.
6. Measured with load shown in *Figure 10 on page 19*.
7. ICCO2 is the maximum average load current that the device can supply to memory in the battery backup mode.

Table 10. Crystal electrical characteristics (externally supplied)

Symbol	Parameter[1][2]	Min	Typ	Max	Unit
f_O	Resonant frequency		32.768		kHz
R_S	Series resistance			60	kΩ
C_L	Load capacitance		12.5		pF

1. These values are externally supplied. STMicroelectronics recommends the KDS DT-38: 1TA/1TC252E127, Tuning Fork Type (thruhole) or the DMX-26S: 1TJS125FH2A212, (SMD) quartz crystal for industrial temperature operations. KDS can be contacted at kouhou@ kdsj.co.jp or http://www.kdsj.co.jp for further information on this crystal type.
2. Load capacitors are integrated within the M41T315Y/V/W. Circuit board layout considerations for the 32.768kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.

Figure 11. Power down/up mode AC waveforms

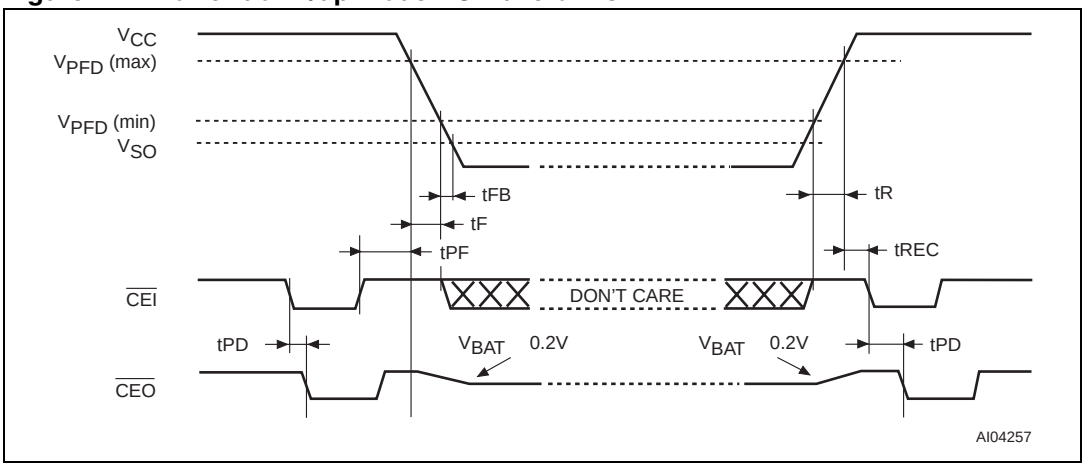


Table 11. Power down/up trip points DC characteristics

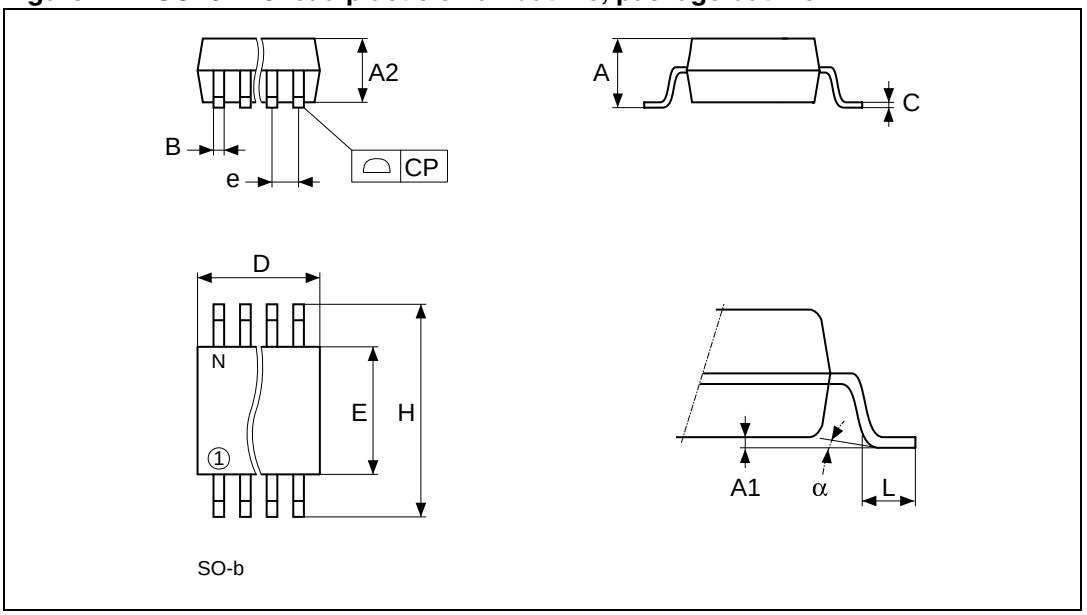
Symbol	Parameter[1][2]		Min	Max	Unit
t_{REC}	V_{PFD} (max) to $\overline{CEI}$ low		1.5	2.5	ms
t_F	V_{PFD} (max) to V_{PFD} (min) V_{CC} fall time		300		µs
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} fall time		10		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} rise time		0		µs
t_{PF}	$\overline{CEI}$ high to power-fail		0		µs
t_{PD}[3][4]	$\overline{CEI}$ propagation delay	M41T315Y		10	ns
		M41T315V/W		15	ns

1. Valid for ambient operating temperature: TA = –40 to 85°C; VCC = 4.5 to 5.5V or 2.7 to 3.6V (except where noted).
2. Measured at 25°C.
3. Measured with load shown in *Figure 10 on page 19*.
4. Input pulse rise and fall times equal 10ns

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 12. SO16 - 16-lead plastic small outline, package outline

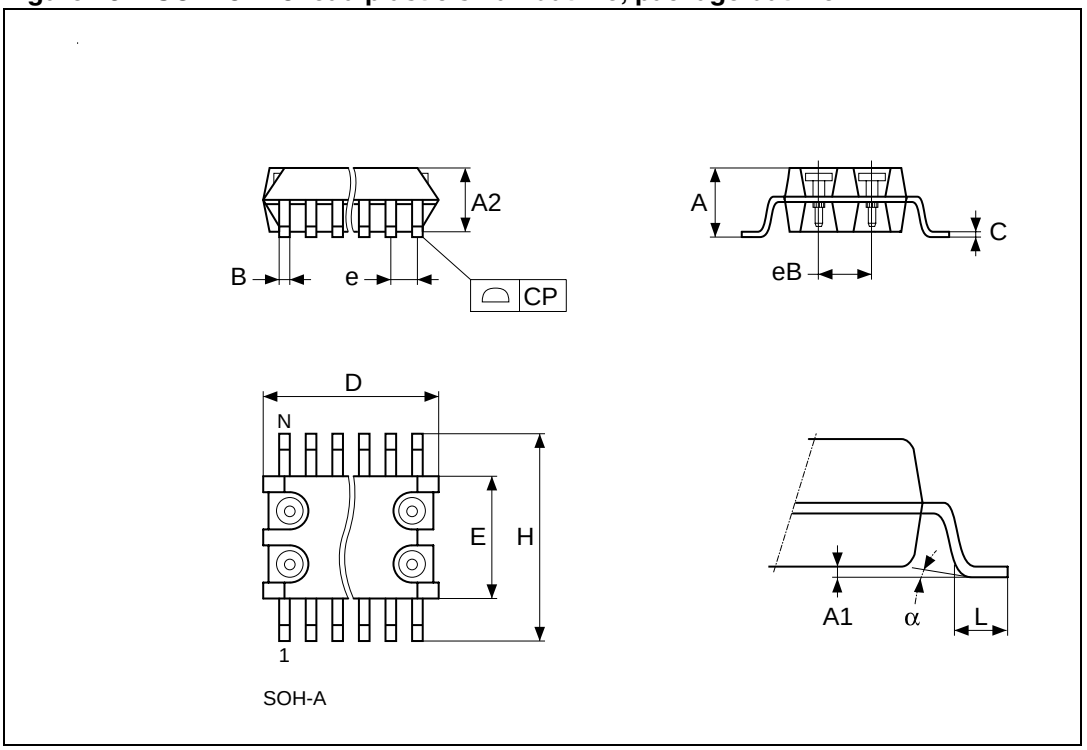


Note: Drawing is not to scale

Table 12. SO16 - 16-lead plastic small outline (150 mils body width), package mechanical data

Sym	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2			1.60			0.063
B		0.35	0.46		0.014	0.018
C		0.19	0.25		0.007	0.010
D		9.80	10.00		0.386	0.394
E		3.30	4.00		0.150	0.158
e	1.27	-	-	0.050	-	-
H		5.80	6.20		0.228	0.244
L		0.40	1.27		0.016	0.050
a		0°	8°		0°	8°
N	16			16		
CP			0.10			0.004

Figure 13. SOH28 - 28-lead plastic small outline, package outline



Note: Drawing is not to scale.

Table 13. SOH28 - 28-lead plastic small outline, package mechanical data

Sym	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.12
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	-	-	0.050	-	-
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
a		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

Figure 14. SH - 4-pin SNAPHAT housing for 48mAh battery and crystal, package mechanical data

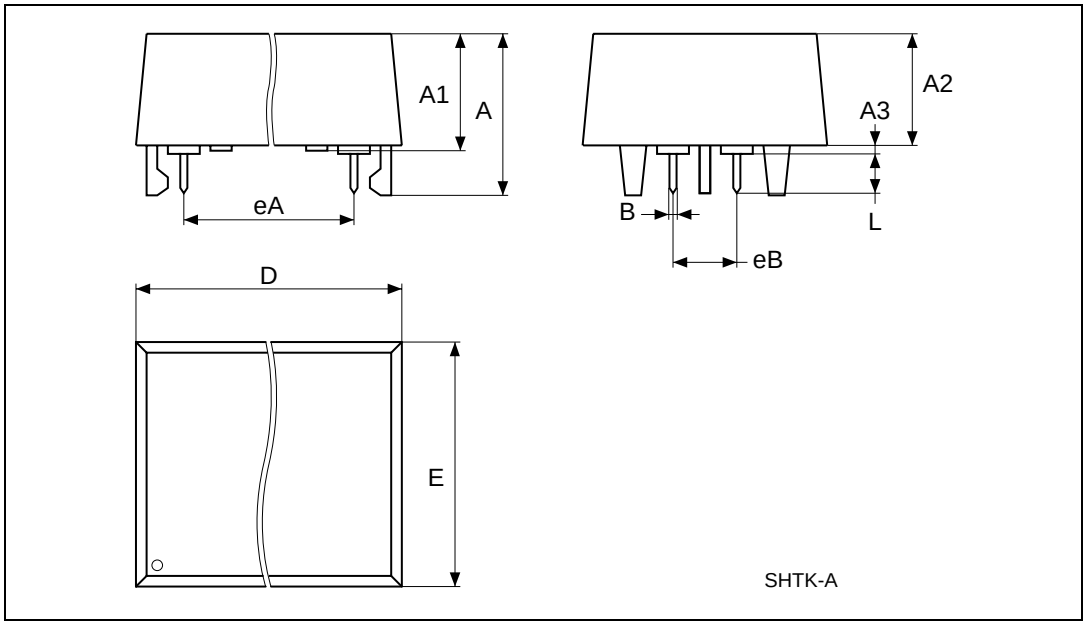


Table 14. SH - 4-pin SNAPHAT housing for 48mAh battery and crystal, package mechanical data

Sym	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78		0	0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38		0	0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

Figure 15. SH - 4-pin SNAPHAT housing for 120mAh battery and crystal, package outline

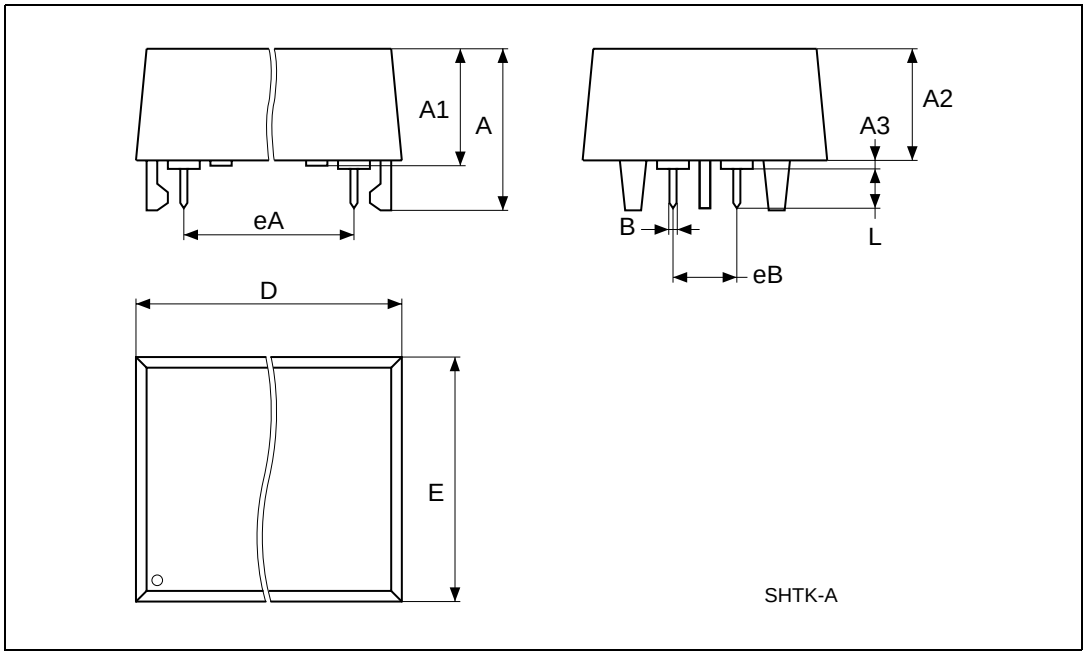


Table 15. SH - 4-pin SNAPHAT housing for 120mAh battery and crystal, package mechanical data

Sym	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54		0	0.415
A1		8.00	8.51		0.315	0.335
A2		7.24	8.00		0.285	0.315
A3			0.38		0	0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	0.710
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

7 Part numbering

Table 16. Ordering information scheme

Example: M41T 315Y –65 MH 6 E

Device type

M41T

Supply voltage and write protect voltage

315Y(1) = V_{CC} = 4.5 to 5.5V; V_{PFD} = 4.25 to 4.50V

315V = V_{CC} = 3.0 to 3.6V; V_{PFD} = 2.80 to 2.97V

315W = V_{CC} = 2.7 to 3.3V; V_{PFD} = 2.60 to 2.70V

Speed

–65 = 65ns (315Y)

–85 = 85ns (315V/W)

Package

MH(2) = SOH28

MQ = SO16

Temperature range

6 = –40 to 85°C

Shipping method

For SOH28:

blank = Tubes (not for new design - use E)

E = Lead-free package (ECOPACK®), tubes

F = Lead-free package (ECOPACK®), tape & reel

TR = Tape & reel (not for new design - use F)

For SOH16:

blank = Tubes (not for new design - use E)

E = Lead-free package (ECOPACK®), tubes

F = Lead-free package (ECOPACK®), tape & reel

TR = Tape & reel (not for new design - use F)

1. Contact local sales office
2. The SOIC package (SOH28) requires the SNAPHAT® battery package which is ordered separately under the part number "M4Txx-BR12SHX" in plastic tube or "M4TXX-BR12SHXTR" in tape & reel form (see *Table 17 on page 28*).

Caution: Do not place the SNAPHAT battery package “M4TXX-BR12SH” in conductive foam as it will drain the lithium button-cell battery.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

Table 17. SNAPHAT battery table

Part number	Description	Package
M48T28-BR12SH	Lithium battery (48mAh) SNAPHAT	SH
M48T32-BR12SH	Lithium battery (120mAh) SNAPHAT	SH

8 Revision history

Table 18. Document revision history

Date	Revision	Changes
Jun-2001	1.0	First issue
17-Jul-2001	1.1	Basic formatting changes
18-Sep-2001	1.2	Changed pin 8 in 28-pin to V_{SS}
27-Sep-2001	1.3	Added ambient temp to DC characteristics table (*Table 9*)
01-May-2002	1.4	Modify reflow time and temperature footnote (*Table 6*)
04-Nov-2002	1.5	Modify crystal electrical characteristics table footnotes (*Table 10*); add marketing status (*Table 16*)
26-Mar-2003	1.6	Update test condition (*Table 9*)
08-Jun-2004	2.0	Reformatted; add lead-free information
26-Nov-2007	3	Reformatted document; product status Not for New Design; added lead-free second level interconnect information to cover page and *Section 6: Package mechanical data*; updated *Table 6*.

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